

**Bachelor of Science (Honours)**

**in**

**Microelectronics with Embedded Technology**

**(RMB2)**

**Title:**

General Purpose Timer (TIM2 to TIM5)

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# CHAPTER 1: INTRODUCTION

## 1.1 Objective:

- To study the theory of general purpose timer (TIM2).

- To configure the TIM2 and investigate the result of different configuration on Timer 2 (TIM2).

## 1.2 Brief Background:

The general-purpose timers consist of a 32-bit auto-reload counter driven by a programmable prescaler. They may be used for a variety of purposes, including measuring the pulse lengths of input signals (input capture) or generating output waveforms (output compare and PWM).

Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds using the timer prescaler and the RCC clock controller prescalers. The timers are completely independent, and do not share any resources. They can be synchronized together. The TIMx timers are linked together internally for timer synchronization or chaining. When one Timer is configured in Master Mode, it can reset, start, stop or clock the counter of another Timer configured in Slave Mode. Figure 1 presents an overview of the trigger selection and the master mode selection blocks.

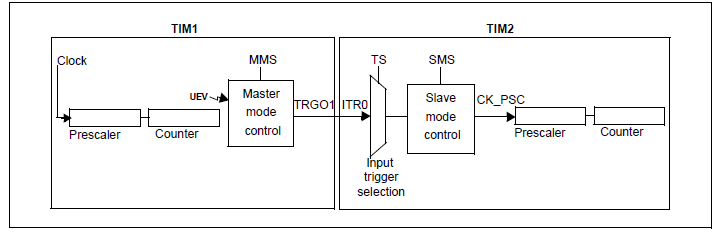


Figure 1: Overview of the trigger selection and the master mode selection blocks.

The main features of general-purpose TIM2 timer included:

1. 32-bits up, down, up/down auto-reload counter.
2. 16-bits programmable prescaler used to divide the counter clock frequency by any factor between 1 and 65536.
3. Up to 4 independent channels for (Input capture, output compare, PWM generation, one-pulse mode output).
4. Synchronization circuit to control the timer with external signals and to interconnect several timers.
5. Interrupt/DMA generation on the following event (update, trigger event, input capture, output compare).
6. Supports incremental (quadrature) encoder and hall-sensor circuitry for positioning purposes.
7. Trigger input for external clock or cycle-by-cycle current management.

The general-purpose timer block diagram was shown in figure 2.

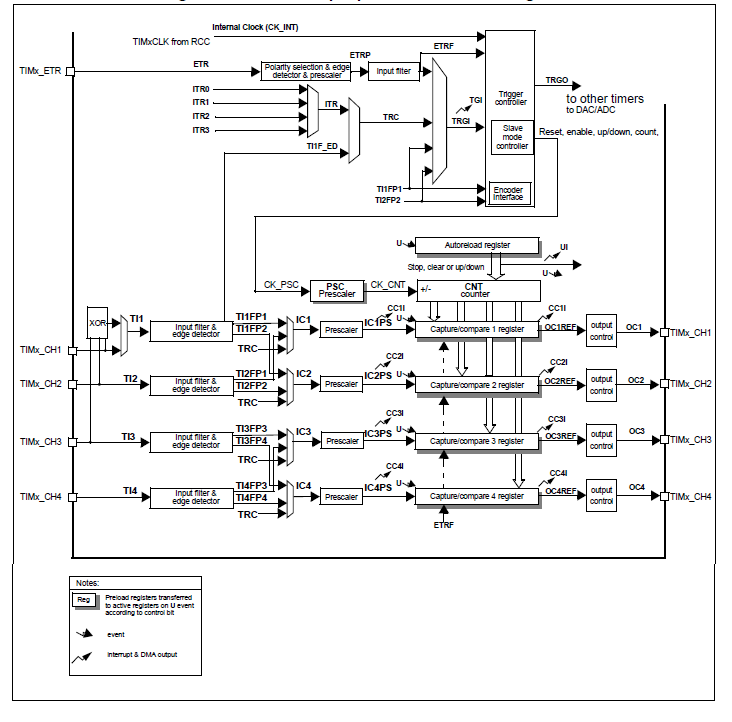


Figure 2: General-purpose timer block diagram

# CHAPTER 2: METHODOLOGY

Three features were configured and investigate in this experiment, which included basic timer mode, output compare mode and input capture mode. Basic timer mode can used to investigate the behavior of counter with different configurations. Output compare mode used to compare the counter value to the register value then create a trigger signal to form a different clock cycle, the result had been capture by using oscilloscope. In input capture mode, the register are used to latch the value of the counter after a transition detected by the corresponding input signal.

## 2.1 Basic counter mode:

The main block of the TIM2 is a 32-bit counter with its related auto-reload register, when the counter count up until it reached the value that loaded into auto-reload register, the counter will restart and count up again (if the timer is not in one-pulse mode). The counter clock can be divided by a prescaler to change the period of the clock. The counter, auto-reload register and the prescaler register can be read or write by the software even when the counter is running. Thus the three time base unit that needed to program included counter register (TIM2\_CNT), prescaler register (TIM2\_PSC) and auto-reload register (TIM2\_ARR).

Preload enable bit (ARPE) in TIM2\_CR1 register control whether the content of auto-reload register transferred into the shadow register permanently or at each update event (UEV). UEV is sent when the counter reached the overflow in upcounting mode or underflow in downcounting mode. Besides that, the counter is clocked by the prescaler output and the prescaler can divide the counter clock frequency by any factor between 1 and 65536.

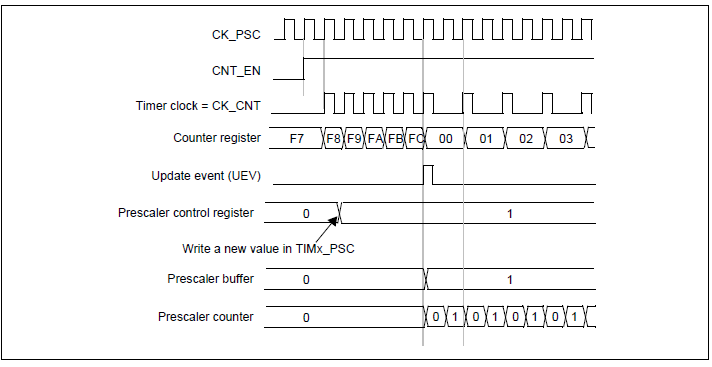


Figure 3: Counter timing diagram with the prescaler division changed from 1 to 2.

To investigate the behaviour of the counter, the following procedure was done:

1. RCC was configure and the clock of TIM2 was enabled.
2. GPIO pin was configure as the output of counter.
3. TIM2\_CNT, TIM2\_PSC and TIM2\_ARR was configured with different data.
4. The result was captured by using oscilloscope.

Besides the time base unit, there are three different mode in counter, which is up-counting, down-counting and centre-aligned mode. Up-counting mode allow counter to count up until value in ARR then restart the counter from 0. Down-counting mode start the counter from the value in ARR and count down to 0 then restart the counter from the value in ARR. Centre aligned mode slightly more complicated, it start counting up from 0 until value of ARR then count down until 0 then start count up again and repeat the counting.

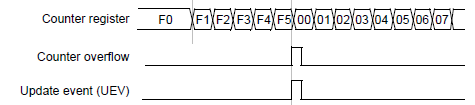


Figure 4: example of up-counting mode.

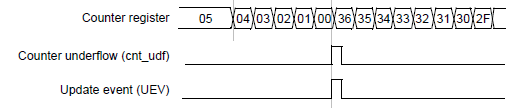


Figure 5: example of down-counting mode.

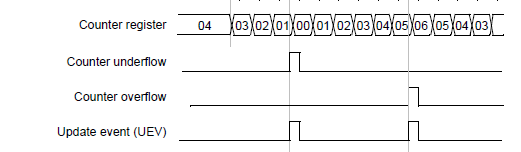


Figure 6: example of center-aligned mode.

## 2.2 Output mode:

There are three different mode that can be configured in output mode, which included forced output mode, output compare mode and pulse width modulation (PWM) mode.

***Forced output mode:***

In output mode, each output compare signal can be forced to active or inactive level directly by software without the comparison between the output compare register and the counter, this is called forced output mode. To force an output compare signal to its active level, the OC1M bits in TIM2\_CCMR1 register was program as 101 thus oc1ref is forced high and OC1 get opposite value to CC1P polarity. Besides that, oc1ref signal can be forced low by writing the OC1M bits to 100 in the TIM1\_CCMR1 register.

However, the comparison between the TIM1\_CCR1 shadow register and the counter is still performed and allows the flag to be set. Thus the interrupt and DMA requests can be sent accordingly.

***Output Compare mode:***

This mode is used to control an output waveform or indicating when a period of time has elapsed. The counter will keep compare to the value of the shadow register, when a match is found, the output compare function will assign the corresponding output pin to a programmable value defined by the output compare mode and the output polarity. Then a flag (CC1IF) in interrupt status register will be set and an interrupt will be generated if the corresponding interrupt mask is set.

In output compare mode, the update event UEV that will be generated when timer overflow has no effect on oc1ref and OC1 output. It is because oc1ref and OC1 output were only affected by comparison between shadow register and the counter. To investigate this mode, the following procedure was done:

1. Counter clock was selected as internal clock.
2. The desired date was written in the TIM2\_ARR and TIM2\_CCR1 registers.
3. TIM2\_CCMR1 register was configured to set channel 1 as output mode.
4. The counter was enabled by setting CEN bit in TIM2\_CR1 register.

TIM2\_CCR1 register can be updated at any time to control the output waveform, the example is shown in figure 7.

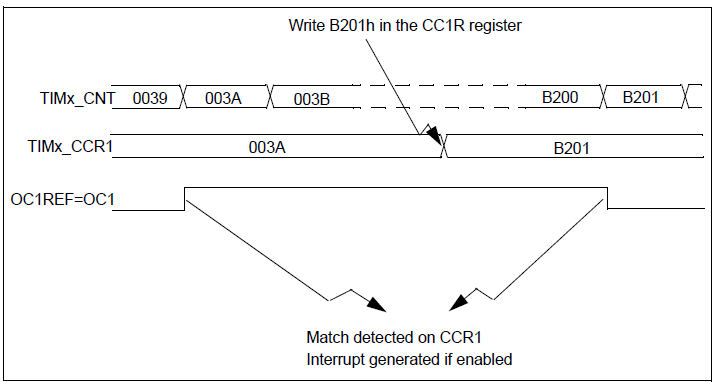


Figure 7: Output compare mode, toggle on OC1

***PWM mode:***

Pulse width modulation mode allow the generation of a signal with a frequency determined by value of TIM2\_ARR register and a duty cycle determined by the value of the TIM2\_CCR1 register.

Pulse width modulation mode allows you to generate a signal with a frequency determined

by the value of the TIMx\_ARR register and a duty cycle determined by the value of the

TIMx\_CCRx register.

The PWM mode can be selected independently on each channel (one PWM per OCx

output) by writing 110 (PWM mode 1) or ‘111 (PWM mode 2) in the OCxM bits in the

TIMx\_CCMRx register. You must enable the corresponding preload register by setting the

OCxPE bit in the TIMx\_CCMRx register, and eventually the auto-reload preload register by

setting the ARPE bit in the TIMx\_CR1 register.

As the preload registers are transferred to the shadow registers only when an update event

occurs, before starting the counter, you have to initialize all the registers by setting the UG

bit in the TIMx\_EGR register.

OCx polarity is software programmable using the CCxP bit in the TIMx\_CCER register. It

can be programmed as active high or active low. OCx output is enabled by the CCxE bit in

the TIMx\_CCER register. Refer to the TIMx\_CCERx register description for more details.

In PWM mode (1 or 2), TIMx\_CNT and TIMx\_CCRx are always compared to determine

whether TIMx\_CCRx≤TIMx\_CNT or TIMx\_CNT≤TIMx\_CCRx (depending on the direction

of the counter). However, to comply with the ETRF (OCREF can be cleared by an external

event through the ETR signal until the next PWM period), the OCREF signal is asserted