

**Bachelor of Science (Honours)**

**in**

**Microelectronics with Embedded Technology**

**(RMB2)**

**Title:**

General Purpose Timer (TIM2 to TIM5)

**Name ：**Ng Yen Aeng

**ID Number ：**15WAU09632

**Lecturer**: Dr. Poh Tze Ven

**Course**: BAME2123 Microcontroller Peripherals

# CHAPTER 1: INTRODUCTION

## 1.1 Objective:

- To study the theory of general purpose timer (TIM2).

- To configure the TIM2 and investigate the result of different configuration on Timer 2 (TIM2).

## 1.2 Brief Background:

The general-purpose timers consist of a 16-bit or 32-bit auto-reload counter driven by a programmable prescaler. They may be used for a variety of purposes, including measuring the pulse lengths of input signals (input capture) or generating output waveforms (output compare and PWM).

Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds using the timer prescaler and the RCC clock controller prescalers. The timers are completely independent, and do not share any resources. They can be synchronized together. The TIMx timers are linked together internally for timer synchronization or chaining. When one Timer is configured in Master Mode, it can reset, start, stop or clock the counter of another Timer configured in Slave Mode. Figure 1 presents an overview of the trigger selection and the master mode selection blocks.

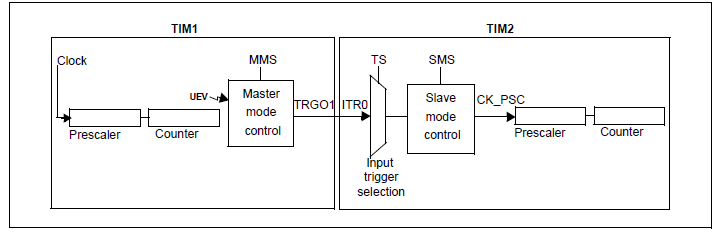


Figure 1

The main features of general-purpose TIM2 timer included:

1. 32-bits up, down, up/down auto-reload counter.
2. 16-bits programmable prescaler used to divide the counter clock frequency by any factor between 1 and 65536.
3. Up to 4 independent channels for (Input capture, output compare, PWM generation, one-pulse mode output).
4. Synchronization circuit to control the timer with external signals and to interconnect several timers.
5. Interrupt/DMA generation on the following event (update, trigger event, input capture, output compare).
6. Supports incremental (quadrature) encoder and hall-sensor circuitry for positioning purposes.
7. Trigger input for external clock or cycle-by-cycle current management.

The general-purpose timer block diagram was shown in figure 2.

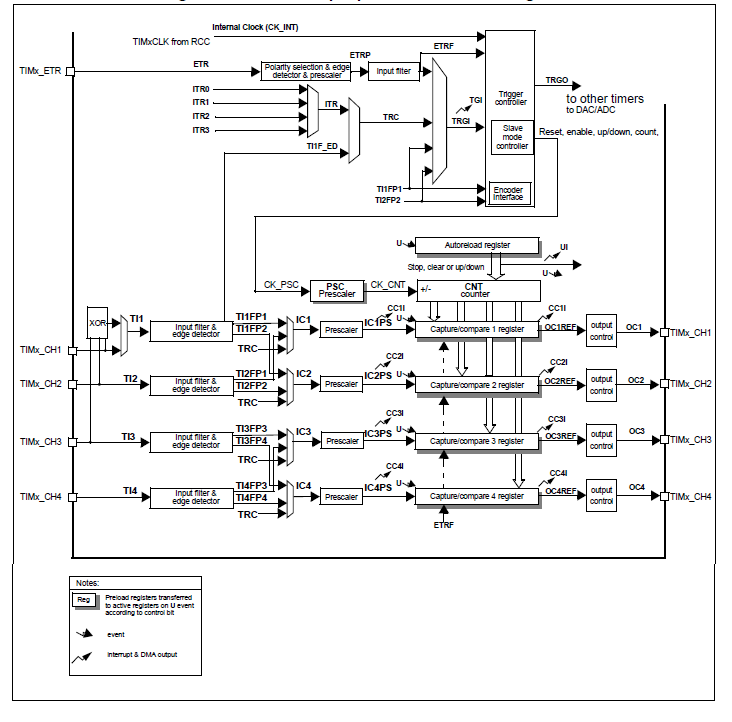


Figure 2

# CHAPTER 2: METHODOLOGY

Three features were configured and investigate in this experiment, which included basic timer mode, output compare mode and input capture mode. Basic timer mode can used to investigate the behavior of counter with different configurations. Output compare mode used to compare the counter value to the register value then create a trigger signal to form a different clock cycle. In input capture mode, the register are used to latch the value of the counter after a transition detected by the corresponding input signal.

## 2.1 Basic counter mode: